

XTRX™ Connectors Pinout



XTRX Mini-PCI Express Card Connector Pinout (rev.3 only)

Pin#	Function	I/O, Pwr	Description	Refer PCI-E pin
1	WAKE#		N/C	
2	+3.3V	Pwr	Main Power Input +3.3V	*A9, A10
3	1PPSI_GPIO1	I (I/O)	External 1PPS input (GPIO1), CMOS 3.3V	
4	GND	Pwr	GND	
5	1PPSO_GPIO2	O (I/O)	GPS 1PPS output (GPIO2), CMOS 3.3V	
6	+1.5V		N/C	
7	CLKREQ#	I	Tied to GND through resistor 330 Ohm.	
8	UIM_PWR	O	UIM_PWR, +1.8V/3.3V	
9	GND	Pwr	GND	
10	UIM_DATA	I/O	UIM DATA, CMOS 1.8V/3.3V	
11	REF_CLK-	I	PCI Express Reference clock differential pair signal	A14
12	UIM_CLK	O	UIM CLOCK, CMOS 1.8V/3.3V	
13	REF_CLK+	I	PCI Express Reference clock differential pair signal	A13
14	UIM_RESET	O	UIM RESET, CMOS 1.8V/3.3V	
15	GND	Pwr	GND	
16	UIM_VPP		N/C	
17	TDD_GPIO3	O (I/O)	TDD TX Enable control output (GPIO3), CMOS 3.3V	
18	GND	Pwr	GND	
19	MHZ_IN	I	**External TCXO Clock Input, CMOS 1.8V/3.3V	
20	GPIO4	I/O	GPIO4, CMOS 3.3V	
21	GND	Pwr	GND	
22	PERST#	I (I/O)	PERST# input (GPIO in case of USB), CMOS 3.3V	*A11
23	PERn0	O	PCI Express Receiver differential pair signal	A17
24	+3.3Vaux		N/C	
25	PERp0	O	PCI Express Receiver differential pair signal	A16
26	GND	Pwr	GND	
27	GND	Pwr	GND	
28	+1.5V		N/C	
29	GND	Pwr	GND	
30	MHZ_OUT	O	**Jumper to CMOS 1.8V/3.3V output. N/C by default.	
31	PETn0	I	PCI Express Transmitter differential pair signal	B15
32	SMB_DATA		N/C	
33	PETp0	I	PCI Express Transmitter differential pair signal	B14
34	GND	Pwr	GND	
35	GND	Pwr	GND	
36	USB_DM	I/O	USB Negative Data. USB2 compatible.	
37	GND	Pwr	Jumper to GND. Connected by default.	
38	USB_DP	I/O	USB Positive Data. USB2 compatible.	
39	PERp1	O	PCI Express Receiver differential pair signal	A22
40	GND	Pwr	GND	
41	PERp1	O	PCI Express Receiver differential pair signal	A21
42	LED_WWAN#	O (I/O)	***Output for LED (GPIO6). CMOS 3.3V.	
43	GND	Pwr	Jumper to GND. Connected by default.	
44	LED_WLAN#	O (I/O)	***Output for LED (GPIO7). CMOS 3.3V.	
45	GND	Pwr	Jumper to GND. Not Connected by default.	
46	LED_WPAN#	O (I/O)	***Output for LED (GPIO8). CMOS 3.3V.	
47	PETn1	I	PCI Express Transmitter differential pair signal	B20
48	+1.5V		N/C	
49	PETp1	I	PCI Express Transmitter differential pair signal	B19
50	GND	Pwr	GND	
51	GND	Pwr	Jumper to GND. Not Connected by default.	
52	+3.3V	Pwr	Main Power Input +3.3V	*A9, A10

Standard Mini-PCI Express Card Connector Pinout (For reference only)

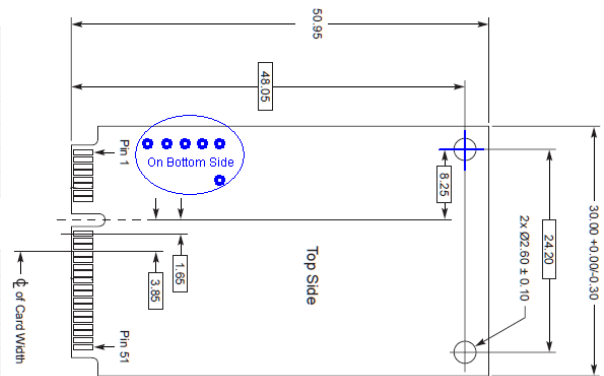
Pin#	Function	I/O, Pwr	Description
1	WAKE#	O	WAKE
2	+3.3V	Pwr	Input +3.3V
3	Reserved		Reserved
4	GND	Pwr	GND
5	Reserved		Reserved
6	+1.5V	Pwr	Input +1.5V
7	CLKREQ#	O	CLKREQ#
8	UIM_PWR	O	UIM_PWR
9	GND	Pwr	GND
10	UIM_DATA	I/O	UIM_DATA
11	REF_CLK-	I	PCI Express Reference clock
12	UIM_CLK	O	UIM CLOCK
13	REF_CLK+	I	PCI Express Reference clock
14	UIM_RESET	O	UIM RESET
15	GND	Pwr	GND
16	UIM_VPP	O	UIM VPP
17	Reserved		Reserved
18	GND	Pwr	GND
19	Reserved		Reserved
20	Reserved		Reserved
21	GND	Pwr	GND
22	PERST#	I	PERST#
23	PERn0	O	PCI Express Receiver differential pair signal
24	+3.3Vaux	Pwr	+3.3V auxiliary
25	PERp0	O	PCI Express Receiver differential pair signal
26	GND	Pwr	GND
27	GND	Pwr	GND
28	+1.5V	Pwr	Input +1.5V
29	GND	Pwr	GND
30	SMB_CLK	I	SMB serial CLOCK
31	PETn0	I	PCI Express Transmitter differential pair signal
32	SMB_DATA	I/O	SMB serial DATA
33	PETp0	I	PCI Express Transmitter differential pair signal
34	GND	Pwr	GND
35	GND	Pwr	GND
36	USB_DM	I/O	USB Negative Data
37	Reserved		Reserved
38	USB_DP	I/O	USB Positive Data
39	Reserved		Reserved
40	GND	Pwr	GND
41	Reserved		Reserved
42	LED_WWAN#	O	LED Output
43	Reserved		Reserved
44	LED_WLAN#	O	LED Output
45	Reserved		Reserved
46	LED_WPAN#	O	LED Output
47	Reserved		Reserved
48	+1.5V	Pwr	+1.5V Input
49	Reserved		Reserved
50	GND	Pwr	GND
51	Reserved		Reserved
52	+3.3V	Pwr	Input +3.3V

JTAG Connector Pinout (Pads on Bottom for Spring Contacts)

Pin#	Function	I/O, Pwr	Description	Placement ****
1	TMS	I	TMS	X-40, Y+1 mm
2	TDI	I	TDI	X-38, Y+1 mm
3	TDO	O	TDO	X-36, Y+1 mm
4	TCK	I	TCK	X-34, Y+1 mm
5	GND	Pwr	GND	X-32, Y+1 mm
6	VCC	Pwr	** Internal Bus Supply +1.8V/3.3V	X-32, Y-4 mm

U.FL Connectors (On Top Side)

Ref	Function	I/O, Pwr	Description	Placement ****
X1	Tx1	O	Transmitting Output 1	X+0.5, Y-5 mm
X2	Tx2	O	Transmitting Output 2	X-5, Y-0 mm
X3	Rx1	I	Receiving Input 1	X-11, Y-20 mm
X4	Rx2	I	Receiving Input 1	X+0.5, Y-12.5 mm
X5	GPS_ANT	I, Pwr	Active GPS Antenna input, +3V/0.1A supply source.	X-41.5, Y+1 mm
X6	CLK_OUT	O	** Int. Clock 30.72 MHz output, CMOS +1.8V/3.3V	X-27, Y+1 mm
X7	CLK_IN	I	** Ext. Clock input, CMOS +1.8V/3.3V	X-22.5, Y+1 mm



The drawing is for reference only.

- *) May require extra components
- **) CMOS 3.3V by default. Depends of Internal BUS I/O assembly variant: 1.8V or 3.3V.
- ****) Do not connect directly to LED, requires a proper current limiting resistor.
- *****) Refer to Upper Mounting Hole (Same side as pin 1 of mPCIe connector).

rev.07_05.2017